REMARKS

Present Status of the Application

The Office Action rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by Horan et al. (U. S. Patent 5,892,964; hereinafter Horan). Applicant has amended claims 1, 10, and 13. After entry of the amendments, claims 1-15 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Claim Rejections under 35 USC 102

The Office Action rejected claims 1-15 under 35 U.S.C. 102(b) as being anticipated by Horan. Applicant respectively traverses the rejections for at least the reasons set forth below.

As discussed in previous Response, Horan failed to disclose the bridge 230 and the extended bus 245 (see FIG. 2). In addition, the bridge is coupled to the control chip 200 by the ABP I 220 but not directly coupled to the control chip 200. The bridges 230, 250 of the present invention allows the extended but to be coupled for extension.

In independent claims 1, 10, and 13, the above features are clearly recited. ***The amendments do not raise new issue.*** Actually, the first AGP is coupled to the control chip set. However, in order to reply the Office Action (pages 5-6), the further amendments have been added. In other words, the first bridge is used to coupled with the AGP bus and the first extended bus. The first bridge does not need to be coupled with the CPU.

In re Horan (Fig. 4A), ***the core logic 104 (control chip) is disclosed and considered by the Office Action as the first bridge*** (Page 5 in Office Action). Applicant respectfully disagrees.

With respect to claims 1, 10, and 13, it should be noted that the core logic 104 is known as the control chip. However, Horan clearly fails to disclose the extension structure, including the bridge 230 and the extended bus 245, and the bridge 230 is coupled to the control chip 200 via the AGP I 220, as recited in independent claims 1, 10, and 13 (se i.e. FIG 2). The core logic 104 does not equivalently disclose the first bridge of the invention. Even though the core logic 104 can be directly coupled with the AGP, the core logic 104 is directly coupled with the CPU for actual operation. On the contrary, the first bridge of the invention is used for extend the bus. The core logic 104 of Horan does not equivalently disclose the main AGP controller of the invention.

Particularly, the core logic 104 of Horan (col. 11, lines) comprises CPU host bus interface and queues 202, memory interface and control 204, host/PCI bridge 206... This means that the core logic 104 is directly operated with the CPU and the Host.

Further with respect to claims 2, 4, 10 and 13, the main AGP controller 310 (see FIG 3) in the first bridge 230 is a device coupled to the first AGP bus for controlling the transmitting and receiving data. The core logic 104 of Horan does not disclose the actual design of the bridge of the invention, which is not directly coupled with the control chipset or the CPU in operation.

The logic chip set 218a (see Fig. 3) or 218c (see Fig. 3A) of Horan is not the additional bridge but is the control chip set, which directly coupled with the CPU, the system memory, and the main PCI bus.

Further still, with respect to claims 5, 12, and 14, with the second bridge 250 can be further included for extending the bus 265. Horan failed to disclose these features.

For at least the foregoing reasons, Applicant respectfully submits that independent claims 1, 10, and 13 patently define over the prior art, and should be allowed. For at least the same reasons, dependent claims 2-9, 11-12, and 14-15 patently define over the prior art as well.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the invention patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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